## What is claimed is:

1	1.	Apparatus comprising:
2		a control point processor;
3		an interface device operatively connected to said control point processor and
4	havi	ng:
5		a semiconductor substrate;
6		a plurality of interface processors formed on said substrate, the number of
7		said processors being at least five;
8		internal instruction memory formed on said substrate and storing instructions
9		accessibly to said interface processors;
8 199 10 1 F 12 13 13 13 13 13 13 13 13 13 13 13 13 13		internal data memory formed on said substrate and storing data passing
15		through said device accessibly to said interface processors; and
12		a plurality of input/output ports formed on said substrate;
13		at least one of said input/output ports connecting said internal data
		memory with external data memory;
1 <b>4</b> 1 <b>5</b>		/ at least two other of said input/output ports exchanging data passing
16 17		through the interface device with an external network under the
17		direction of said interface processors;
18		said control point processor cooperating with said interface device by loading into
19	said	instruction memory instructions to be executed by said interface processors in
20	direc	ting the exchange of data between said data exchange input/output ports and the flow
21	of da	ata through said data memory.
1	2.	Apparatus according to Claim 1 further comprising:
2		a second interface device operatively connected to said control point processor and

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a semiconductor substrate;

having:

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5	a plurality of interface processors formed on said substrate, the number of
6	said processors being at least five;
7	internal instruction memory formed on said substrate and storing instructions
8	accessibly to said interface processors;
9	internal data memory formed on said substrate and storing data passing
10	through said device accessibly to said interface processors; and
11	a plurality of input/output ports formed on said substrate;
12	at least one of said input/output ports connecting said internal data
13	memory with external data memory;
14	at least two other of said input/output ports exchanging data passing
15	through the interface device with an external network under the
	direction of said interface processors;
17	said control point processor copperating with said second interface device by
18	loading into said instruction memory instructions to be executed by said interface
19	processors in directing the exchange of data between said data exchange input/output
20	ports and the flow of data/through said data memory.
<b>₩</b> ••••••••••••••••••••••••••••••••••••	3. Apparatus according to Claim 1 further comprising
2	a second control point processor;
3	said interface device being operatively connected to one of said control point
4	processor and said second control point processor;
5	a second interface device operatively connected to the other of said control point
6	processor and said second control point processor and having:
7	a semiconductor/substrate;
8	a plurality of interface processors formed on said substrate, the number of
9	said processors being at least five;
10	internal instruction memory formed on said substrate and storing instructions
11	accessibly to said interface processors;
12	internal data memory formed on said substrate and storing data passing
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13	through said device accessibly to said interface processors; and
14	a plurality of input/output ports formed on said substrate;
15	at least one of said input/output ports connecting said internal data
16	memory with external data memory;
17	at least two other of said input/output ports exchanging data passing
18	through the interface device with an external network under the
19	direction of said interface/processors;
20	said other control point processor cooperating with said second interface device by
21	loading into said instruction memory instructions to be executed by said interface
22	processors in directing the exchange of data between said data exchange input/output
23	ports and the flow of data through said data memory.
	4. Apparatus according to Claim/1 wherein said control point processor is located
2	remotely from said interface device and is operatively connected thereto through said two
	other input/output ports.
	5. Apparatus comprising:
2	a housing;
3	a backplane mounted in the housing;
4	a plurality of printed circuit board devices mounted in said backplane;
5	circuit elements on one of said circuit board devices comprising:
6	a control point processor;
7	a semiconductor substrate;
8	an interface device operatively connected to said control point processor and
9	having:
10	a plurality of interface processors formed on said substrate, the
11	number of said processors being at least five;
12	internal instruction memory formed on said substrate and storing

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13		instructions accessibly to said interface processors;
14		internal data memory formed on said substrate and storing data
15		passing through said device accessibly to said interface processors;
16		and /
17		a plurality of input/output ports formed on said substrate;
18		at least one of said input/output ports connecting said internal
19		data memory with external data memory;
20		at least two other of said input/output ports exchanging data
21		passing through the interface device with an external network
22		under the direction of said interface processors;
23		said control point processor cooperating with said interface device by loading
24	into	said instruction memory instructions to be executed by said interface
25	proce	ssors in directing the exchange of data between said data exchange
22 25 25 25 25 25 25 25 25 25 25 25 25 2	input/	output ports and the flow of data through said data memory.
	6. Appa	ratus according to Claim 5 wherein said control point processor is formed on
יישיים איים וריים	said semico	nductor substrate.
1	7. Appa	ratus according to Claim 5 further comprising:
2	circuit	elements on a second of said circuit board devices comprising:
3		an interface device operatively connected to said control point processor and
4		having:
5		a semiconductor substrate;
6		a plurality of interface processors formed on said substrate, the
7		number of said processors being at least five;
8		internal instruction memory formed on said substrate and storing
9		instructions accessibly to said interface processors;

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10		internal data memory formed on said substrate and storing data
11		passing through said device accessibly to said interface processors;
12		and /
13		a plurality of input/output ports/formed on said substrate;
14		at least one of said input/output ports connecting said internal
15		data memory with external data memory;
16		at least two other of said input/output ports exchanging data
17		passing through the interface device with an external network
18		under the direction of said interface processors;
19		said control point processor copperating with said interface device by loading
20		into said instruction memory instructions to be executed by said interface
21		processors in directing the exphange of data between said data exchange
22		input/output ports and the flow of data through said data memory.
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ţ	8.	Apparatus comprising:
		a printed circuit board device; and
3		circuit elements mounted on said circuit board device comprising:
4		a control point processor; and
5		an interface device operatively connected to said control point processor and
6		having:
7		a semiconductor substrate;
8		a plurality of interface processors formed on said substrate, the
9		number of said processors being at least five;
10		internal instruction memory formed on said substrate and storing
11		instructions accessibly to said interface processors;
12		internal data memory formed on said substrate and storing data
13		passing through said device accessibly to said interface processors;
14		and
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15		a plurality of input/output ports formed on said substrate;
16		at least one of said input/output ports connecting said internal
17		data memory with external data memory;
18		at least two other of said input/output ports exchanging data
19		passing through the interface device with an external network
20		under the direction of said interface processors;
21		said control point processor cooperating with said interface device by loading
22		into said instruction memory instructions to be executed by said interface
23		processors in directing the exchange of data between said data exchange
24		input/output ports and the flow of data through said data memory.
	9.	Apparatus comprising:
2		a printed circuit board device; and
3		circuit elements mounted on said circuit board device comprising:
24 1 1 1 1 2 3 4 5 5 6 7 6 8		a control point processor;/
5		an interface device operatively connected to said control point processor and
6		having:
7		a semiconductor/substrate;
8		a plurality of interface processors formed on said substrate, the
9		number of said processors being at least five;
10		internal instruction memory formed on said substrate and storing
11		instructions accessibly to said interface processors;
12		internal data memory formed on said substrate and storing data
13		passing through said device accessibly to said interface processors;
14		and /
15		a plurality $\phi$ f input/output ports formed on said substrate;
16		at least one of said input/output ports connecting said internal
17		data memory with external data memory;
18		at/least two other of said input/output ports exchanging data
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passing through the interface device with an external network under the direction of said interface processors;

said control point processor cooperating with said interface device by loading into said instruction memory instructions to be executed by said interface processors in directing the exchange of data between said data exchange input/output ports and the flow of data through said data memory; and

a self routing switching fabric device operatively connected to said interface device and directing data inbound to the apparatus from identifiable addresses to flow outbound from the apparatus to identified addresses.

10. A method comprising the steps of:

storing in an instruction memory instructions for the handling of data transiting an interface device;

executing in a plurality of interface processors the instructions stored in the instruction memory;

receiving a data flow inbound through an input port;

communicating the data flow through the plurality of interface processors; and directing the data flow outbound through an output port in accordance with the execution of the instructions by the interface processors.

- 11. A method according to Claim 10 further comprising parsing the data flow into a plurality of portions, storing selected portions of the parsed data flow in data memory, and directing other selected portions of the parsed data flow to a switching fabric for determination of an outbound direction.
- 12. A method according to Claim 11 further comprising recombining the stored and other selected portions of the data flow prior to direction of the data flow outbound through an output port.

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A method according to Claim 10 wherein the step of communicating the data flow 13. through the plurality of interface processors comprises parsing the data flow into portions and distributing the parsed portions among the plurality of interface processors for handling in parallel.